REMARKS

Claims 1-33 are pending in the application. Please cancel claims 31-33, without prejudice or disclaimer.

Claims 1-33 stand rejected variously under 35 U.S.C. 102(b) or 35 U.S.C. 103(a) in view of U.S. Patent No. 5,852,608 to Dinwiddie, Jr. et al. ("Dinwiddie"), U.S. Patent No. 5,784,699 to McMahon et al. ("MacMahon"), and U.S. Patent No. 5,546,554 to Young et al. ("Young"). In view of the amendments and remarks herein, Applicant respectfully traverses the rejections and asks that they be withdrawn. Applicant believes the amendments place pending claims 1-30 in condition for allowance.

Claims 1-30

The office action asserted that column 11, line 66 of Dinwiddie teaches that the computer system is configured so that control accesses from the CPU are directed to the multiported memory, and that Fig. 1, Ref. 10 teaches that the computer system is configured so that data accesses from the CPU are directed to the main memory.

Applicant still sees no teaching or suggestion in Dinwiddie that control accesses or data accesses are treated at all differently from each other in Dinwiddie. That is, Applicant finds nothing in Dinwiddie that corresponds to directing a

control access to the multiported memory, and directing a data access to the CPU. Instead, data accesses and control accesses appear to be treated the same in Dinwiddie.

Rather than providing a multi-ported memory for more efficient control/status accesses, dual port random access storage mechanism 22 of Dinwiddie provides a data transfer interface between the microprocessor bus 16 and the host processor channel bus 8. (See column 4, lines 59-63 of Dinwiddie). As such, "Data passing from the channel bus 8 to the microprocessor bus 16 or vice versa is at least temporarily stored in this storage mechanism." (See column 4, lines 63-66 of Dinwiddie). That is, dual port random access storage mechanism 22 performs the function of (at least temporarily) storing all data (data and status information) being transferred between the peripherals and the CPU.

Therefore, dual port random access storage mechanism 22 does not perform the same function as the multi-ported memory of the current application and does not provide the same benefits (e.g., avoiding the bus snoop and its attendant delay for control/status accesses and reducing the traffic on the channel between the CPU and the main memory).

Applicant has amended claim 1 to recite a particular implementation that is clearly different than Dinwiddie.

Claim 1 now explicitly recites that control accesses from the central processing unit are "directed to the multi-ported memory and not to the main memory," while data accesses from the central processing unit are "directed to the main memory and not to the multi-ported memory."

According to amended claim 1, not only are control accesses and data accesses directed differently, control accesses are explicitly directed to the multi-ported memory and not to the main memory, while data accesses are explicitly directed to the main memory and not to the multi-ported memory.

In contrast, Dinwiddie teaches that all data being transferred between peripheral devices and the CPU (e.g., data and status information) is stored in the dual ported memory. For example, column 11, line 66 of Dinwiddie teaches that "Considering first the case of DPC operations, each DPC read type command enables a 2-byte word of data or status information to be transferred from the I/O controller 2 to the host processor 1."

Further, it appears that any modification of Dinwiddie to direct control and data accesses differently would render Dinwiddie unsatisfactory for its intended purpose. When a proposed modification would render the prior art invention being modified unsatisfactory for the intended purpose, then there is

no suggestion or motivation to make the proposed modification (see MPEP 2143.01). Dual port storage 22 would no longer function as a data transfer interface between the microprocessor bus and the host processor channel bus for all data. Since Dinwiddie describes this data transfer interface as "A primary feature of the new and improved I/O controller 2," (see column 4, lines 59-60 of Dinwiddie), there is no motivation to modify Dinwiddie to direct data accesses and control/status accesses differently.

Applicant believes that the amendments to claim 1 clearly differentiate claim 1 from Dinwiddie and place claim 1 in condition for allowance.

Independent claims 10, 14, 19, 23, and 27 have been amended to include similar features. Therefore, Applicant believes that each independent claim is now in condition for allowance.

Claims 2-9, 11-13, 15-18, 20-22, 24-26, and 28-30 depend from the independent claims noted above. Therefore, Applicant believes that each of the dependent claims is now in condition for allowance.

Information Disclosure Statement

Applicant notes that the Form PTO-1449 filed with the Information Disclosure Statement on January 5, 2001, has not been initialed and returned. Applicant requests that the

Examiner consider the references filed with the IDS and return the initialed Form PTO-1449 as soon as possible.

CONCLUSION

In view of the amendments and remarks herein, Applicant believes that claims 1-30 are in condition for allowance. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-5070.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 2/7/03

Linda G. Gunderson
Reg. No. 46,341

PTO Customer Number 20985
Fish & Richardson P.C.
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

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